Highly Linear CMOS RF MMIC Amplifier Using Multiple Gated Transistors and its Volterra Series Analysis

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Abstract

CMOS RF MMIC amplifiers are fabricated with linearization technique using multiple gated transistors [6]. At 900 MHz, double and triple gated amplifiers show 2.5 - 4.5 dB larger figure of merit (linearity-DC power consumption), which means that only 1/2 ~ 1/3 of DC power is needed to obtain the same OIP_3 value. Using Volterra series analysis and harmonic balance simulation, it is shown that the linearization technique with the 2nd harmonic termination can increase IIP_3 by amount of 16 dB max. without additional DC power consumption at optimal bias condition, which can reduce more than 90 % of DC power consumption with the same linearity performance.

I. Introduction

These days, the needs for mobile tele communication such as cellular telephone, PCS (personal communication system), GSM (Global System for Mobile Communications), IMT-2000 (International Mobile Telecommunications-2000), etc., are increasing rapidly.

As digital communication is used increasingly, the linearity of an RF amplifier becomes more and more important. Recently, high linearity is required even for LNA's (low noise amplifier), in addition to power amplifiers and driver amplifiers.

To reduce nonlinearity of amplifiers, several linearization methods were developed, and until now, those are used mainly in power amplifier applications[1]-[5]. However, in the case of CDMA transceiver, transmitter and receiver are isolated by means of only duplexer. Because the maximum output power level of power amplifier is around 28 dBm, and the duplexer attenuates only around 40 dB, the spurious signals of transmitter act as main interference sources. These signals fall into the receiver signal band by means of intermodulation and cross-modulation. This is the reason why the linearity requirement of recent LNA is becoming much higher.

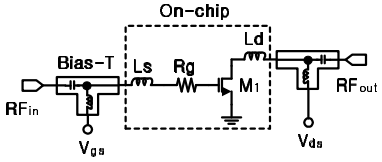
As LNA's and driver amplifiers are being integrated into transceiver chips, the linearity (IP_3) requirement per DC power consumption is getting stringent. To fulfill the linearity specification with minimum power consumption, the need for linearization technique with small power consumption is emerging.

In this paper, RF CMOS MMIC amplifiers are fabricated with linearization technique using multiple gated transistors [6]. In section II, the measurement results of fabricated amplifiers will be given. In section III and IV, CMOS RF amplifiers are analyzed using Voterra series analysis [7],[8]. According to analysis results, IP_3 can be improved further using 2nd harmonic termination. In section V, conclusions will be given.

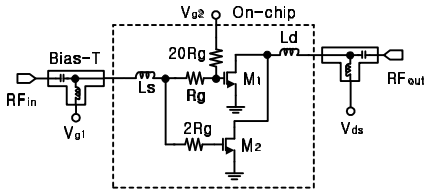
II. Experimental results of single, double and triple gated amplifiers.

Using g_m'' cancellation concept in [6], CMOS MMIC amplifiers are fabricated.

Fig. 1 shows schematics of fabricated CMOS RF amplifiers using multiple gated transistors. Fig. 1 (a) shows conventional common source amplifier, which is named as single gated amplifier (SGA). Fig. 1 (b) and (c) show double gated amplifier (DGA) and triple gated amplifier (TGA), respectively. In those figures, R_g's, $2R_g$'s, and $20R_g$'s act as stabilization resistors and bias circuit simultaneously. V_{ds} is 3 V, V_{th} is 0.8 V for all amplifiers.



(a) schematic of single gated amplifier (SGA)



(b) schematic of double gated amplifier (DGA)

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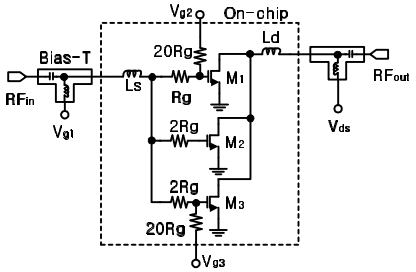

(c) schematic of triple gated amplifier (TGA)

Fig. 1 Schematic of fabricated amplifiers.

Fig. 2 shows measured g_m'' of SGA, DGA, and TGA. As shown in that figure, magnitudes of g_m'' of TGA is decreased significantly at the V_{gs} range of 0.8 ~ 1.4 V.

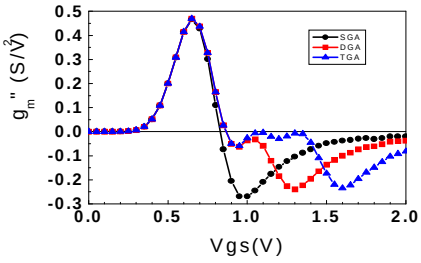

Fig. 2 Measured g_m'' of SGA, DGA, and TGA

Measured OIP_3 vs. V_{gs} graph is in Fig. 3. Here, applied input RF power is –20 dBm, and used input RF frequencies are 900 MHz and 901 MHz. DGA and TGA have 4.5 dB and 2.5 dB max. larger OIP_3 than SGA, respectively.

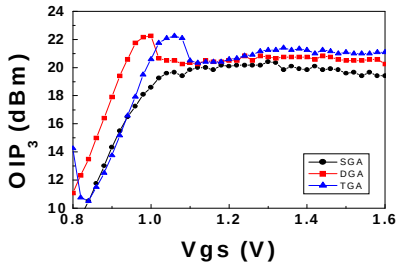

Fig. 3 Measured OIP_3 of fabricated amplifiers.

In mobile application, it is required to obtain high OIP_3 with smaller DC power consumption. A figure of merit (F.O.M.) concerning linearity and DC power consumption can be defined as

$$F.O.M. = 10\log\left[\frac{OIP_3(mW)}{P_{DC}(mW)}\right](dB) \qquad (1)$$

where P_{DC} is DC power consumption. This value compares linearity of circuits at the same DC power consumption condition.

Fig. 4 shows F.O.M. of fabricated amplifiers. SGA has optimal values around V_{th} + 0.2 V, which means that V_{gs} of conventional common source MOSFET amplifier should be set around this value to obtain high linearity with minimum DC power consumption. DGA and TGA increased these optimal values by amount of 4.5 dB and 2.5 dB max., respectively. In the case of DGA, 4.5 dB higher F.O.M. means that only 1/3 of DC power is needed to obtain the same OIP_3 value.

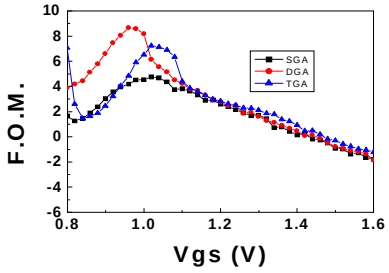

Fig. 4. Measured F.O.M. of fabricated amplifiers.

Fig. 5 shows measured fundamental output power and IMD_3 of fabricated amplifiers as input power varies. IMD_3 suppression effect continues to P_{1dB} power level.

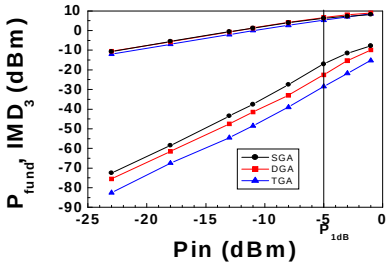

Fig. 5 P_{fund} and IMD_3 vs. input power.

III. Nonlinear Volterra series analysis of CMOS RF amplifiers and its application to multiple gated amplifiers.

In section II, the importance of g_m'' is shown. In this section, using Volterra series analysis, other nonlinear factors will be investigated, which affect total linearity of CMOS amplifier. Fig. 6 shows analyzed model of conventional common source amplifier. In this figure, C_{gs}, C_{gd}, g_m, C_{ds}, etc. have nonlinear characteristics as V_{gs} and V_{ds} varies. Considering only g_m nonlinearity, IIP_3 is calculated. [7], [8]. Other component values except g_m, is assumed to be constant at a given bias condition, and then only the effect of g_m nonlinearity is analyzed.

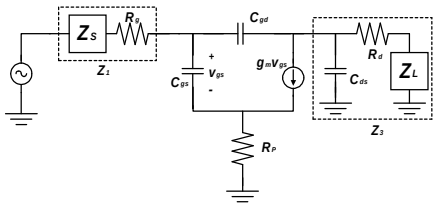

Fig. 6 The used equivalent model of common source amplifier.

g_m nonlinearity is considered upto the 3rd order as

$$i_{DS} = I_{DC} + g_1 v_{gs} + g_2 v_{gs}^2 + g_3 v_{gs}^3 \quad (2)$$

$$where, g_1 = g_m, g_2 = \frac{1}{2!} g_m', g_3 = \frac{1}{3!} g_m''$$

Equations in the previous work for BJT [7] are converted to be adequate for MOSFET case, and the results are;

$$IIP_3(2\omega_a - \omega_b) = \frac{1}{6\,\mathrm{Re}[Z_S(\omega)] \cdot |H(\omega)| \cdot |A_1(\omega)|^3 |\varepsilon(\Delta\omega, 2\omega)|} \quad (3)$$

$$H(\omega) = \frac{1 + j\omega C_{gs}[Z_1(\omega) + R_P] + j\omega C_{gd} Z_1(\omega)}{g_1 - j\omega C_{gd}[1 + R_P(g_1 + j\omega C_{gs})]} \quad (4)$$

$$A_1(\omega) = \frac{1}{g_1 + g(\omega)} \cdot \frac{1 + j\omega C_{gd} Z_3(\omega)}{Z_x(\omega)} \quad (5)$$

$$\varepsilon(\Delta\omega, 2\omega) = g_3 - g_{OB} \quad (6)$$

$$g_{OB} = \frac{2g_2^2}{3}\left[\frac{2}{g_1 + g(\Delta\omega)} + \frac{1}{g_1 + g(2\omega)}\right] \quad (7)$$

$$g(\omega) = \frac{1 + j\omega C_{gd}[Z_1(\omega) + Z_3(\omega)] + j\omega C_{gs}[Z_1(\omega) + Z_x(\omega)]}{Z_x(\omega)} \quad (8)$$

$$Z_x(\omega) = R_P + j\omega C_{gd}[Z_1(\omega) R_P + Z_1(\omega) Z_3(\omega) + R_P Z_3(\omega)] \quad (9)$$

Using these equations, IIP_3 of 600/0.5 NMOS device is calculated, and compared with simulation results using HP ADS harmonic balance simulator with BSIM3v3 MOSFET model. Fig. 7 shows calculation and simulation results of 600/0.5 NMOS device. As shown in that figure, calculation results coincide with simulation result at V_{gs} of smaller than 1.2 V (V_{th} + 0.4 V). From the figure, it can be said that, in this region, only g_m nonlinearity dominates total linearity of CMOS amplifier.

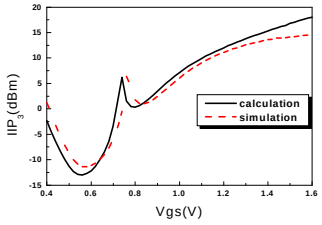

Fig. 7 Calculation and simulation result of 600/0.5 NMOS device.

Above this region, as gm′ and gm″ values become small, another nonlinearity source dominates total linearity of amplifier. Consequently, calculation result deviates from simulation result. However, because this region has optimum figure of merit (linearity-DC power consumption), from now on, fabricated amplifier will be analyzed in this region.

Fig. 8 shows calculation and simulation results of SGA, DGA, and TGA. For all amplifiers, calculation coincides with simulation.

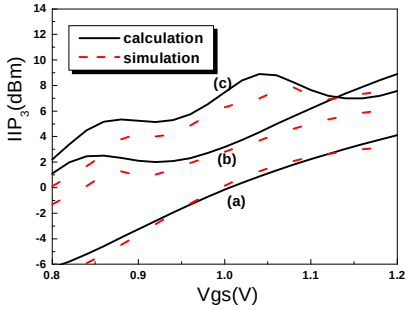

Fig. 8 Calculation and simulation results of (a)SGA, (b)DGA, and (c)TGA.

IV. The effect of 2nd harmonic component on linearity of CMOS amplifier.

In equations (3)-(9), $Z_S(\omega)$, $H(\omega)$, $A_1(\omega)$ are linear transfer function of fundamental frequency, and determined by required gain, noise figure, input/output match, etc. $\varepsilon(\Delta\omega,2\omega)$ value depends on Z_S and Z_L at sub-harmonic frequency ($\Delta\omega$) and the 2nd harmonic frequency (2ω). Fig. 9 shows magnitudes of $\varepsilon(\Delta\omega,2\omega)$, g_3, and g_{OB} term of SGA and TGA in (6). As shown in those figures, in the case of SGA, g_{OB} has comparable value to g_3. However, it is shown

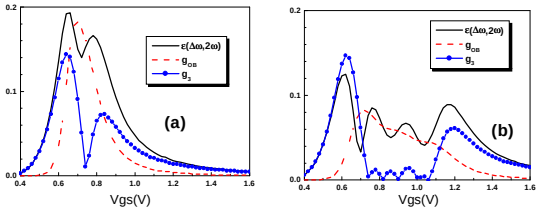

Fig. 9 Magnitudes of g_3, g_{OB}, and $\varepsilon(\Delta\omega,2\omega)$ of (a) SGA and (b) TGA.

that although g_3 is cancelled in TGA significantly, g_{OB} dominates $\varepsilon(\Delta\omega,2\omega)$, in other words, total linearity of TGA. In our case, Z_S ($\Delta\omega$) and $Z_L(\Delta\omega)$ are sufficiently small, and

does not affect ε(Δω,2ω). ε(Δω,2ω) value in the case of Z_S (2ω) or Z_L(2ω) equals zero, is shown in Fig. 10. As shown in that figure, ε(Δω,2ω) is reduced significantly. Z_S (2ω) or Z_L(2ω) value can be made zero using input or output 2nd harmonic termination, and the simulation results are in Fig. 11. As shown in the figure, TGA with the 2nd harmonic termination can increase IIP_3 by amount of 16 dB max. without additional DC power consumption at linearity-optimal-V_{gs}-bias condition, which can reduce more than 90% of DC power consumption with same linearity performance. Fig. 12 shows IMD_3 simulation results of SGA and TGA with/without 2nd harmonic termination.

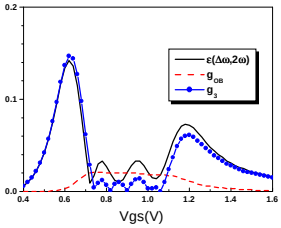

Fig. 10 Magnitudes of g_3, g_{OB}, and ε(Δω,2ω) of TGA in the case of Z_S (2ω) or Z_L(2ω) equals zero.

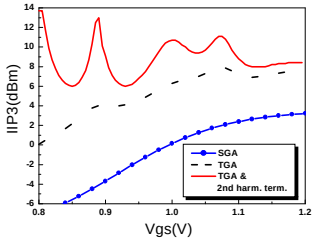

Fig. 11 Simulated IIP_3 of SGA, TGA, and TGA with 2nd harmonic termination

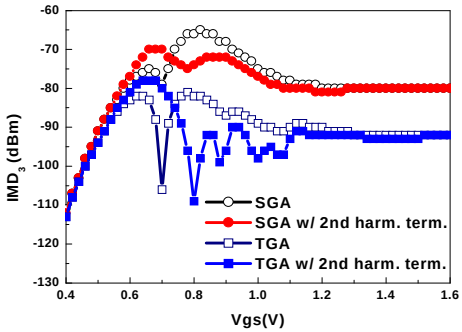

Fig. 12 IMD_3 simulation results of SGA, SGA with 2nd harmonic termination, TGA, and TGA with 2nd harmonic termination.

V. Conclusions

RF CMOS MMIC amplifiers are fabricated with linearization technique using multiple gated transistors. Double and triple gated amplifiers show 2.5 - 4.5 dB larger figure of merit (linearity-DC power consumption).

By Volterra series analysis, it is shown that linearization technique using multiple gated transistors can increase IIP_3 by amount of 16 dB max. and 7 - 10 dB typical without additional DC power consumption at linearity-optimal-V_{gs}-bias condition.

Using the two techniques (multiple gated transistors and the 2nd harmonic termination), it is possible to reduce more than 90 % of DC power consumption with the same IP_3 performance of CMOS RF amplifier.

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